What is claimed is:

Sub A6

1. A semiconductor device provided with a memory cell including a first load transistor, a second load transistor, a first driver transistor, a second driver transistor, a first transfer transistor, and a second transfer transistor, the semiconductor device comprising:

a first conduction type well region;

a second conduction type well region;

a first gate-gate electrode layer including a gate electrode of the first load transistor and a gate electrode of the first driver transistor;

a second gate-gate electrode layer including a gate electrode of the second load transistor and a gate electrode of the second driver transistor;

a first drain-drain wiring layer that forms a part of a connection layer that electrically connects a drain region of the first load transistor and a drain region of the first driver transistor;

a second drain-drain wiring layer that forms a part of a connection layer that electrically connects a drain region of the second load transistor and a drain region of the second driver transistor;

a first drain-gate wiring layer that forms a part of a connection layer that electrically connects the first gate-gate electrode layer and the second drain-drain wiring layer; and

a second drain-gate wiring layer that forms a part of a connection layer that electrically connects the second gate-gate electrode layer and the first drain-drain wiring layer,

wherein the first load transistor and the second load transistor are provided in the first conduction type well region,

wherein the first driver transistor and the second driver transistor are provided in the second conduction type well region,

wherein the second drain-gate wiring layer is located in a layer over the first drain-gate wiring layer, and has an upper layer of the second drain-gate wiring layer and a lower layer of the second drain-gate wiring layer,

wherein the upper layer is located in a layer over the lower layer, and

wherein the upper layer is provided above one of the first conduction type well region and the second conduction type well region.

2. The semiconductor device according to claim 1,

wherein the upper layer is provided above the second conduction type well region without exceeding a border between the first conduction type well region and the second conduction type well region.

3. The semiconductor device according to claim 2, further

comprising a main word line,

wherein the main word line is provided in the same layer as the upper layer, and is provided above the first conduction type well region without exceeding a border between the first conduction type well region and the second conduction type well region.

4. The semiconductor device according to claim 1,

wherein the upper layer is provided above the first conduction type well region without exceeding a border between the first conduction type well region and the second conduction type well region.

5. The semiconductor device according to claim 4, further comprising a main word line,

wherein the main word line is provided in the same layer as the upper layer, and is provided above the second conduction type well region without exceeding a border between the first conduction type well region and the second conduction type well region.

6. The semiconductor device according to claim 1,

wherein the first drain-gate wiring layer is electrically connected to the second drain-drain wiring layer through a contact section,

wherein the lower layer is electrically connected to the second gate-gate electrode layer through a contact section, and

wherein the upper layer is electrically connected to the first drain-drain wiring layer and the lower layer through contact sections, respectively.

7. The semiconductor device according to claim 1,

wherein the first gate-gate electrode layer, the second gate-gate electrode layer and the first drain-gate wiring layer are provided in the same layer, and

wherein the first drain-gate wiring layer is provided over a border between the first conduction type well region and the second conduction type well region.

8. The semiconductor device according to claim 1,

wherein the first drain-gate wiring layer and the upper layer are provided in a manner not to overlap one another as viewed from a vertical direction.

9. The semiconductor device according to claim 1,

wherein the first gate-gate electrode layer, the second gate-gate electrode layer and the first drain-gate wiring layer are located in a first conductive layer,

wherein the first drain-drain wiring layer, the second drain-drain wiring layer and the lower layer are located in a second conductive layer, and

wherein the upper layer is located in a third conductive layer.

10. The semiconductor device according to claim 1, wherein a second conductive layer is a nitride layer of a refractory metal.

11. The semiconductor device according to claim 1, wherein a second conductive layer has a thickness of 100 to 200nm.

12. A ~~memory~~ system provided with the semiconductor device according to any one ~~of~~ claims 1 to 11.

13. An electronic apparatus provided with the semiconductor device according to any one of claims 1 to 11.